LumiFree™ Application Note

AN-LF-001-S1: Wiring Integration Supplement

Detailed Wiring Specifications for M972A Drive Board Integration

Item	Details
Document Number	AN-LF-001-S1
Parent Document	AN-LF-001 Version 1.0
Source Reference	PWB_UNIT_M972A Specification Rev. 1.0 (July 2025)
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Applicable Products	LumiFree LAM020 and LAM041 with M972A Drive Board

1. Introduction

1.1 Purpose

This supplement provides detailed wiring and electrical integration specifications for the M972A drive board used with LumiFree™ electrically tunable light shaping panels. The information herein is derived from the JDI PWB_UNIT_M972A engineering specifications and is intended to assist lighting fixture designers with hardware integration.

1.2 Scope

This document covers:

- M972A drive board connector locations and pin orientations
- Wiring connections from M972A to LumiFree LC panels via interface boards
- Mating connector specifications for custom harness fabrication
- Extended electrical characteristics and absolute maximum ratings
- I²C communication timing and protocol overview
- Power-on sequence and timing requirements

1.3 Parent Document

This supplement accompanies LumiFree™ Application Note AN-LF-001 (Integration Guide for LED Lighting Fixtures). Users should refer to AN-LF-001 for complete system architecture, optical design guidelines, thermal management, control implementation, and troubleshooting information.

In case of any conflict between this supplement and AN-LF-001, the parent document takes precedence unless explicitly noted otherwise.

1.4 Terminology Note

The following terminology clarifications apply to this document and referenced JDI specifications:

- "Relay board" in some JDI diagrams refers to the Interface Board (also called Connector Board) in GRE Alpha documentation. These terms are interchangeable.

2. M972A Drive Board Hardware Overview

2.1 Basic Specifications

Parameter	Specification
Product Name	LumiFree Drive Board
Product Number	M972A
Size	45.0 × 45.0 × 6.7 mm (Typ.)
Weight	7 ± 0.7 g
Operating Temperature	-20°C to +70°C (no condensation)
Storage Temperature	-20°C to +80°C (no condensation)
Applicable Product	GRE Alpha LumiFree LAM020 and LAM041

2.2 Board Layout and Connector Locations

The M972A drive board features three main connectors for system integration. The following diagram shows the physical location of each connector and the pin 1 orientation.

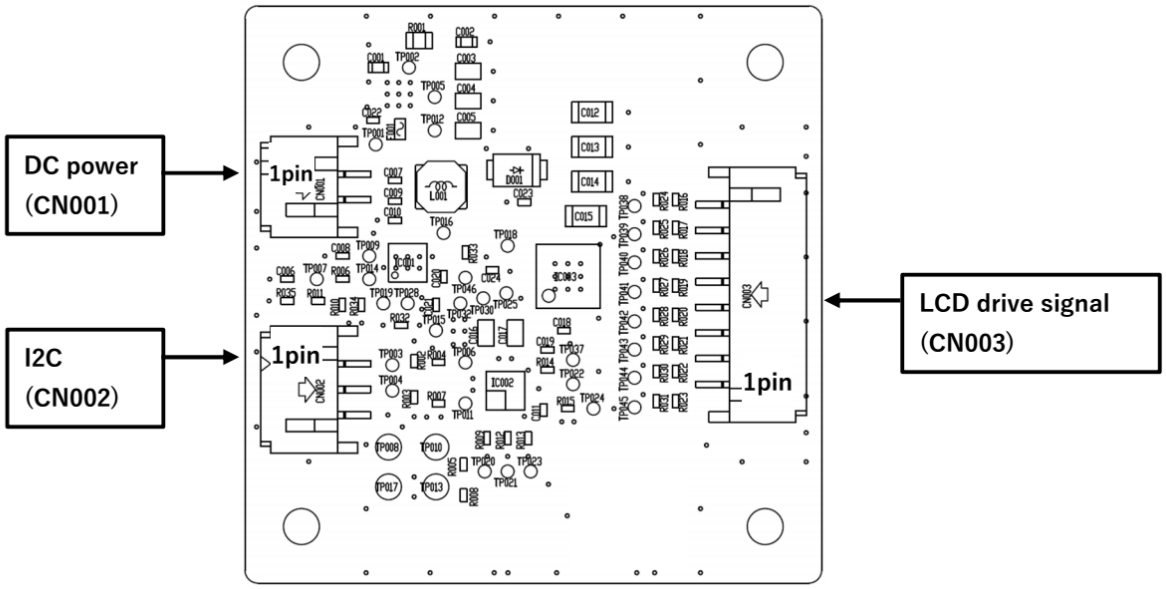

Figure 2.1: M972A Drive Board Connector Locations and Pin 1 Orientation (see connector summary table 2.3)

2.3 Connector Summary

Connector	Function	Pins	Description
CN001	DC Power Input	2	Power supply connection (VCC and GND)
CN002	I²C Control	3	I²C communication (SCL, SDA, GND)
CN003	LC Drive Output	8	LC panel drive signals (AMPOUT1-8)

3. Wiring Connections

3.1 M972A to LumiFree Panel Connection Diagram

The following diagram illustrates the complete wiring path from the M972A drive board to the LumiFree LC panels. Each M972A can drive up to four LC panels using two interface boards.

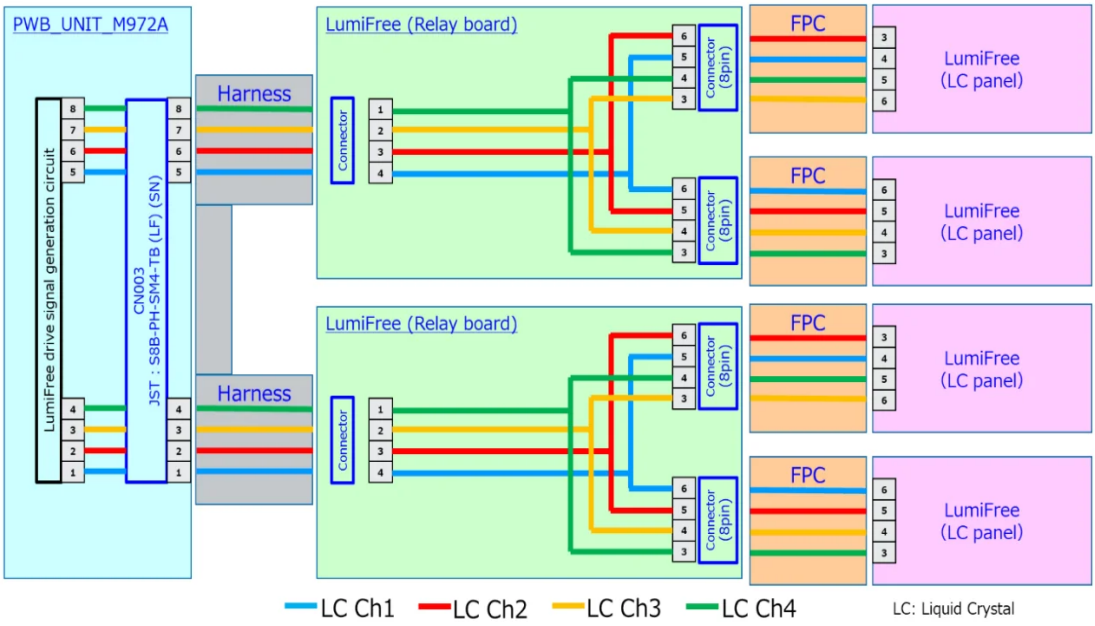

Figure 3.1: M972A to Interface Board to LC Panel Wiring Connection Diagram

> ***Terminology:*** *The "Relay board" shown in the above diagram is referred to as "Interface Board" or "Connector Board" within this and other GRE Alpha documentation.*

3.2 Connection Overview

The M972A drive board connects to LumiFree LC panels through interface boards using the following signal path:

Signal Flow:

M972A (CN003) → Harness → Interface Board → FPC Cable → LC Panel

Channel Assignments:

- LC Ch1 (Cyan): Controls one LC element zone
- LC Ch2 (Red): Controls one LC element zone
- LC Ch3 (Yellow): Controls one LC element zone
- LC Ch4 (Green): Controls one LC element zone

3.3 CN003 Pin Assignments

Pin	Symbol	Function	I/O	Remarks
1	AMPOUT1	LC Ch1 signal	O	
2	AMPOUT2	LC Ch2 signal	O	
3	AMPOUT3	LC Ch3 signal	O	
4	AMPOUT4	LC Ch4 signal	O	
5	AMPOUT5	LC Ch1 signal	O	
6	AMPOUT6	LC Ch2 signal	O	
7	AMPOUT7	LC Ch3 signal	O	
8	AMPOUT8	LC Ch4 signal	O	

3.4 Panel Configurations

- Pins 5-8 (AMPOUT5-8) → First Interface Board → 2 LC panels
- Pins 1-4 (AMPOUT1-4) → Second Interface Board → 2 LC panels

Note: *Connect M972A board and LumiFree (Interface board) in a way that the pins of each LC Ch1-4 are aligned. Even if the interface board connections are crossed during assembly, there will be no problem in operation or quality.*

4. Connector Specifications

4.1 Mating Connector Part Numbers

For custom harness fabrication, the following mating connectors are recommended. All connectors are manufactured by J.S.T. MFG. CO., LTD. (JST PH series).

M972A Connector	Board-Side Part Number	Mating Housing
CN001 (Power)	S2B-PH-SM4-TB(LF)(SN)	PHR-2
CN002 (I²C Control)	S3B-PH-SM4-TB(LF)(SN)	PHR-3
CN003 (LC Output)	S8B-PH-SM4-TB(LF)(SN)	PHR-8

4.2 CN001 Power Connector Pinout

Pin	Symbol	Function	I/O/P
1	VCC	Power supply	P
2	GND	Ground	P

4.3 CN002 I²C Control Connector Pinout

Pin	Symbol	Function	I/O/P	Remarks
1	SCL	Serial clock	I	Pulled to VCC internally (4.7kΩ)
2	SDA	Serial data	I/O	Pulled to VCC internally (4.7kΩ)
3	GND	Ground	P	

4.4 Wire and Contact Specifications

- Crimp contacts: SPH-002T-P0.5S or equivalent
- Recommended wire gauge: AWG 24-28
- Customers must prepare harnesses based on the connector information provided

Note: *For connector specifications used for LumiFree interface boards, check the specifications of the relevant product and prepare a compatible harness.*

5. Electrical Specifications

5.1 Absolute Maximum Ratings

WARNING: Exceeding absolute maximum ratings may cause permanent damage to the device.

Parameter	Symbol	Min	Max	Unit	Remarks
Power supply voltage	VCC	-0.3	6.0	V	
Input voltage	VI	-0.3	VCC+0.3	V	CN002: SCL, SDA
Output voltage	VO	-0.3	VCC+0.3	V	CN002: SDA

5.2 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage	VCC	-	2.97	-	5.50	V
Power supply ripple	Vp-p	With LumiFree	-	-	200	mVp-p
Power supply current	IVCC	-20°C≤Ta≤70°C	-	-	350	mA
Inrush current	IPEAK	Rising 2V/100μs	-	-	1200	mA
Input voltage high	VIH	-	0.8×VCC	-	VCC	V
Input voltage low	VIL	-	0	-	0.2×VCC	V
Output voltage high	VOH	-	-	-	VCC	V
Output voltage low	VOL	IOL=1.5mA	-	-	0.4	V
Internal pull-up	RI	Ta=25°C	4.465	4.700	4.935	kΩ

Note: *VIH, VIL, and RI apply to CN002 SCL and SDA pins. VOH and VOL apply to CN002 SDA pin. Output is open-drain with internal 4.7kΩ pull-up.*

5.3 Power Supply Capacity Requirements

To ensure product safety, the current supply capacity of the customer's power supply should be either:

- 2A or more (to allow the internal fuse to blow in the event of abnormality), or
- 350mA to 450mA (current-limited supply)

WARNING: Power supplies with intermediate current capacity (450mA to 2A) may not properly trigger internal protection mechanisms in fault conditions.

Fuse Information: *The M972A drive board incorporates an internal fuse (KAMAYA FCC16102ABTP) in the input power path. For this fuse to provide effective overcurrent protection, the customer's power source shall be capable of delivering a minimum fault current of 2 A. Power sources with a maximum current capability of 2 A or less may not permit the fuse to open under certain fault conditions.*

The internal fuse does not provide protection for circuits upstream of its location. For example, in the event of a short circuit at the interface connector (CN001), upstream components such as connectors may overheat and potentially ignite before the fuse opens.

To ensure comprehensive protection, the fixture designer shall implement appropriate upstream protection measures in the system design.

When using an external fuse, its ratings and time-current characteristics must be selected appropriately so that the fuse does not operate unintentionally due to the M972A's normal inrush current (up to 1200 mA).

It is recommended to make the final selection by conducting a verification of the actual system. (Inrush current is highest when both X and Y diffusion are set to maximum.)

5.4 External Pull-up Resistor Considerations

The M972A includes integrated 4.7kΩ pull-up resistors on the I²C bus lines (5% tolerance at 25°C). When designing the customer control system interface:

- If external pull-ups are added, they must reference the same VCC supply as the M972A
- For long cable runs or high bus capacitance, stronger pull-ups (e.g., 2.2kΩ) may improve signal integrity

6. Timing and Sequencing

6.1 Power-On Sequence

The M972A requires specific timing for proper initialization and I²C communication:

Parameter	Symbol	Min	Max	Unit	Remarks
VCC turn on → Init complete	t1	-	150	ms	
VCC turn on → I²C access enable	t2	150	-	ms	Wait before sending commands
VCC turn on → Light source on	t3	150	-	ms	Verify behavior at startup
Light source off → VCC turn off	t4	0	-	ms	
VCC turn off → VCC turn on	t5	500	-	ms	Minimum power cycle time

> ***Important:*** *The rising and falling speed of VCC should be slower than 2V/100μs and faster than 2V/10ms.*

6.2 State Transitions

The M972A operates in two states:

Initializing State:

- Initialization process executes after power-on
- I²C communication from host is NOT accepted
- Maximum duration: 150ms

Normal Mode:

- Accepts I²C communication from host
- LumiFree control performed according to X-diffusion and Y-diffusion settings
- Default values (0x00 for both X and Y) applied until host sets values

6.3 Power Supply Dip Behavior

Normal operation cannot be guaranteed when the power supply dips below VCC(Min.) for a short period (such as a momentary power failure) and then returns to normal voltage. If abnormal operation is observed, restart the system following the ON/OFF sequence timing requirements.

7. I²C Communication Overview

7.1 I²C Specifications

- Device Address: 0x71 (7-bit)
- Sub Address: 0x00
- Mode: Follow Fast mode specifications per NXP UM10204
- Clock stretch function is used

7.2 Diffusivity Write Command

To set the X and Y diffusivity values:

- Send: [Start] [Device Addr + W] [Sub Addr 0x00] [Y diffusivity] [X diffusivity] [Stop]
- Y diffusivity range: 0x00 to 0xFF
- X diffusivity range: 0x00 to 0xFF

Note: *Settings are retained during Normal mode. When power is turned off, settings are lost and default values (0x00) are restored on next startup.*

7.3 Diffusivity Read Command

To read the current X and Y diffusivity values:

- Send: [Start] [Device Addr + W] [Sub Addr 0x00] [Repeated Start] [Device Addr + R]
- Receive: [Sub Addr] [Y diffusivity] [X diffusivity] [NACK] [Stop]

Revision History

Revision	Date	Description	Author
1.0	January 2026	Initial release	GRE Alpha Technical Team

Contact Information

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